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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,580	07/21/2003	Scott B. Herner	MA-040-a	7514

33971 7590 02/22/2006

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,580	HERNER ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,20-27 and 29-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,20-23,25-27 and 29-31* is/are rejected.

7)☒ Claim(s) *24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Argument

1. Applicant's arguments, filed 12/14/2005 with respect to the rejection(s) of claim 24 under Obvious-type Double Patenting have been fully considered and are persuasive. The rejections have been withdrawn. The applicants argue that Hills does not teach a three dimensional memory array disposed at numerous level above a substrate, as required in amended claim 20. This argument is moot in view of the new ground of rejection of claim 20 based on Su and Noble as discussed below

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 25, 27, 30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Su et al (US 5,837,582)

Su discloses a method for forming HSG silicon layer comprises the steps of:

forming a first in-situ doped silicon layer 10 over a substrate material 9 in a LPCVD chamber/pressure chamber while flowing phosphine/precursor gas (col 3, lines 59-62)

forming an undoped polysilicon capping layer 11B on and in contact with layer 10/doped silicon layer without removing the substrate from the chamber and without flowing phosphine/discontinuing precursor gas (col 3, lines 66-67; fig. 3)

etching/removing the undoped capping layer 11B (col 4, lines 36-37; fig. 5)

Su also discloses using the invention to manufacture DRAM device/memory device (col 1, lines 66-65)

The limitation of claim 27 has been discussed above

Regarding claim 30, fig. 3 of Su shows that layer 10/first doped layer is thicker than undoped capping layer 11B.

Regarding claim 31, Su discloses that undoped layer 11B having a thickness of 300-500 angstroms (col 4, lines 1-2)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 20-23, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Su (US 5,837,582) in view of Noble (US 6,306,703)

Su's method has been described above. Unlike the instant claimed inventions as per claims 20, 29, Su fails to specifically disclose forming a three dimension memory array from the silicon layers, the three dimensional memory array comprises memory cells disposed at numerous levels above a substrate

Noble discloses a method for forming a memory array comprises a step of forming a three dimension memory array from the doped and undoped polysilicon layers, the three dimensional memory array comprises memory cells disposed at numerous levels above a substrate 100 (col 9, lines 50-60; fig. 30)

One skilled in the art at the time the invention was made would have found it obvious to employ Su silicon layers to form a three dimension memory array in view of Noble because Noble discloses that the doped silicon layers provide conductive paths to the contact regions of the memory array (col 8, lines 36-40)

Regarding claims 21-22, fig. 3 of Su shows that layer 10/first doped layer is thicker than undoped capping layer 11B. Su discloses that undoped layer 11B having a thickness of 300-500 angstroms (col 4, lines 1-2)

Regarding claim 23, Su discloses forming a doped silicon layer 12/second in-situ doped silicon layer in contact with layer 11 B (col 4, lines 4-6)

6. Claims 2, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Su (US 5,837,582) in view of Hsu (US 6,613,626)

Su's method has been described above. Unlike the instant claimed inventions as per claims 2, 26, Su fails to specifically disclose removing the undoped polysilicon capping layer by CMP

Hsu discloses a method for forming a CMOS comprises the step of removing the undoped polysilicon layer by CMP (col 6, lines 42-47)

One skilled in the art at the time the invention was made would have found it obvious to modify Su method by removing the undoped polysilicon layer by CMP as per Hsu because Hsu discloses that polysilicon needs to be removed by CMP (col 6, lines 46-47)

Allowable Subject Matter

7. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bhardwaj et al (US 6,051,503) discloses that reactive ion etching step and depositing step can be performed in a same chamber (col 6, lines 20-40)

Response to Arguments with respect to the rejection(s) of claims 1, 25

9. Applicant's arguments filed 12/14/2006 have been fully considered but they are not persuasive.

The applicants argue that Su does not teach depositing the undoped capping layer without removing the substrate material from the pressure vessel because Su discloses performing an RIE between deposition of the doped silicon layer and deposition of the undoped capping layer and RIE cannot be performed in a chamber used to deposit silicon, thus, one skilled in the art would assume that the wafer was removed from the pressure vessel between the deposition and etching step. This argument is unpersuasive for the following reasons: Su is totally silent about the wafer being removed from the chamber between the deposition and etching step as shown in col 3, lines 60-67, it is conventional in the art of semiconductor processing to perform reactive ion etching step and depositing steps in a same pressure chamber (see prior art made of record for evidence of this basis). Therefore, the examiner asserts that Su discloses depositing the undoped capping layer without removing the substrate material from the pressure vessel as required by claim 1 and 25

Applicants also argue that undoped capping layer 11b in Su is not removed because Su discloses etching the layer 11b and layer 11b is still present in the finished device. This argument is unpersuasive for the following reason while it is true that layer 11b is still present in the finished device it is also true that claims 1 and 25 do not require completely removing the undoped capping layer from the semiconductor device since fig. 5 of Su clearly shows that portion of capping layer 11b is etched/removed from the semiconductor device, Su teaching of etching/removing portion of undoped capping layer 11b certainly reads on the limitation of "removing the undoped silicon capping layer" as set forth in claims 1 and 25.

In response to applicant's argument that there is no suggestion to combine the references of Su and Hsu because the undoped polysilicon layers of Hsu and Su serving different purpose and the undoped polysilicon layer of Su is not removed, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, since Su discloses removing the undoped polysilicon layer (as discussed above) and the motivation to combine the references comes from Hsu (Hsu teaches using CMP to remove undoped polysilicon), one skilled in the art looking for a teaching to remove undoped polysilicon layer would have found it obvious to employ Hsu teaching in Su method to produce the claimed invention.

10. Applicant's amendment necessitated the new ground(s) of rejection of claims 20-23 presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
February 17, 2006